UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,895	03/24/2004	John R. Humphrey	10354*3	7412

23416 7590 10/24/2006

CONNOLLY BOVE LODGE & HUTZ, LLP
P O BOX 2207
WILMINGTON, DE 19899

EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,895	HUMPHREY ET AL.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *July 27, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on July 17, 2004 was considered by the examiner.

Drawings

3. The drawings are objected to because details of the drawings cannot be read, in particular in Figures 1 and 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites "arranging the plurality of small banks of internal memory so that all data dependencies are capable of being statically wired". It is not apparent that the disclosure shows how the banks must be arranged to read on this limitation, and thus it not apparent to an artisan how to make and use the claimed invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites "arranging the plurality of small banks of internal memory so that all data dependencies are capable of being statically wired". It is not apparent that the disclosure shows how the banks must be arranged to read on this limitation, and thus it not apparent to an artisan what possible arrangements of banks might read on this limitation. Hereinbelow, it will be broadly interpreted as any arrangement with data dependencies that might be statically wired.

7. Claims 1, 2, 8, and 14 recite "the FDTD method" at lines 1 and/or 2, which is unclear because 1) it lacks proper antecedent basis, and 2) it is not apparent if there is only one FDTD method, and if not then to which method is referred. Claims 1, 2, 8, and

14 additionally recite "very high bandwidth", which is a limitation of degree and apparently not defined by the disclosure. Claims 3-7, 9-13, and 15-16 incorporate these limitations by dependency.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Placidi, "A Custom VLSI Architecture for the Solution of FDTD Equations", in view of Kiamilev et al., US 5,951,627.

10. As to claim 1, Placidi discloses a multiple bank memory system for acceleration of the FDTD method and arranging them so that all data dependencies are capable of being statically wired. See Abstract, Figs. 2 and 3, and page 574 at "3. System Architecture." Placidi does not specifically disclose that the memory is dual-port on-chip memory. The advantages of dual-port memory were well known to improve overall performance by allowing two operations in parallel, see Kiamilev Abstract. It would have been obvious to implement the memory banks of Placidi as dual-port to achieve the desirable advantage of improved performance. Additionally, progress in the art is steadily improving the integration of more circuitry into smaller space, which improves speed as well as lowering cost. It would have been obvious to an artisan that integrating the memory of Placidi onto the processor chip would have these

advantages. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use dual-port on-chip memory, because this was taught and known to improve operating performance and lower costs.

11. As to claims 2 and 8, Placidi discloses memory banks (of the SDRAM, Fig. 2) connected to one-cycle delay elements (d's at a, k1, k2, Fig. 3), delay elements connected to computation engines (d's connected to adders/multipliers in Fig. 3), second plurality of banks connected to computation engines (see Fig. 3 at b, c, d, e), computation engines connected to output banks (at y, Fig. 3, see also page 574 at "3. System Architecture").

12. As to claims 3, 4, 5, 9, 10, and 11, since the banks may store any data they handle fields having the directional dependencies as recited.

13. As to claims 6 and 12, the system of Placidi does not indicate there is a bulk storage, but systems routinely have such storage (such as a hard disk) which is used to store the data as recited, and would have been desirable because it was well known to cost effectively stores a large amount of data in a non-volatile manner.

14. As to claims 7 and 13, the system of Placidi is unspecific as to the number of banks but indicates there are a plurality; it would have been within the assumptions of one skilled in the art to assume a specific number such as 6 banks would be included in this amount.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No:

5,497,473 Cache memory banks connected to delay elements.

Non-Patent Literature:

Durbano, et al., "Hardware Implementation of a Three-Dimensional Finite-Difference Time-Domain Algorithm".

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gary J Portka
Primary Examiner
Art Unit 2188

GARY PORTKA
PRIMARY EXAMINER

October 23, 2006